

What is Claimed is:

1. Semiconductor apparatus comprising:

a semiconductor body having a top surface and being of a first conductivity type and including an insulating layer over a portion of the top surface;

a semiconductor region of a second opposite conductivity type adjacent said semiconductor body for forming a p-n junction with the semiconductor body which underlies the insulating layer; and

a plurality of spaced-apart conductive strips each having first and second ends with the first ends at the top surface of the semiconductor body and the second ends buried under the insulating layer, and with the second end of at least one of the conductive strips making low resistance contact with the semiconductor region and at least one failing to make a low resistance contact.

2. The semiconductor apparatus of claim 1 wherein the conductive strips are doped semiconductor material of the second conductivity type.

3. The semiconductor apparatus of claim 2 wherein at least two of the conductive stripes make a low resistance contact to the semiconductor region.

4. Semiconductor apparatus comprising:

a silicon wafer comprising a portion that includes at least one calibration well of the conductivity type opposite that of its surrounding region for forming a vertical p-n junction therewith;

an insulating layer overlying the p-n junction;

a plurality of conductive stripes extending from the top surface of the portion and having buried ends underlying partially the insulating layer for forming distinct conductive paths in said surrounding region and directed at the vertical edge of the p-n junction of which at least one conductive stripe penetrates the junction to form a conductive path to the well and at least one that falls short of the junction; and

at least one other conductive connection to the well for forming a conductive path through the calibration well with a penetrating stripe.

5. A method for locating an edge of a semiconductor well of one conductivity that is formed in a semiconductor body of the opposite conductivity type which edge underlies an insulating layer, said method comprising the steps of:

forming in the semiconductor body before the semiconductor region and the insulating layer are formed a plurality of distinct conductive stripes of each includes a first end at the top surface of the semiconductor body and a second end buried under a portion of the top surface where the insulating layer is to be formed, of which at least one conductive stripe has a second end extends across the edge and at least one second end that be short of the edge;

forming an insulating layer over a portion of the top surface of the semiconductor body and covering the second ends of the stripes;

forming in the semiconductor body a semiconductor well

of the opposite conductivity type for forming the edge that underlies the insulating layer whose edge is to be located, said semiconductor well including the buried second ends of only some but less than all of the conductive stripes; and

5 determining which of the stripes includes buried second ends that make low resistance connections to the semiconductor well.

6. The method of claim 5 in which the different stripes are of different lengths whereby different stripes extend
10 different distances under the insulating layer towards the edge and there are identified the stripes that penetrate the least distance into the semiconductor well from the stripes that make low resistance connection to the well.

7. The method of claim 6 wherein the stripes are of doped
15 semiconductor material.

8. A method for determining in a semiconductor wafer an edge that is of a well of conductivity different from its surrounding region and that underlies an insulating layer that overlies the edge of the well, said method includes forming over
20 the surface before the forming of either the insulating layer or the well an overlay pattern of spaced-apart conductive stripes that extend under the insulating layer to be formed to provide distinct conductive paths in the semiconductor wafer, of which at least one extends sufficiently to penetrate the edge of the well
25 to be formed to provide a low resistance connection to the well after it has been formed.

9. The method of claim 8 in which at least a pair of stripes of said overlay pattern extend into the well whereby a voltage applied between the two stripes of the pair provides a measurable current flow and the location of the buried ends of such stripes serves to locate the position of the edge.

10. The process of claim 9 in which the two stripes penetrate the same edge of the well.

11. The process of claim 10 in which the two stripes penetrate opposing edges of the well.

12. The process of claim 8 in which less than all of the stripes of the overlay pattern penetrate the well.

13. The process of claim 9 in which less than all of the stripes of the overlay pattern penetrate the well.

14. The method of claim 8 in which a voltage bias is applied to the stripes of the overlay pattern to determine which stripes penetrate the edge of the well.

15. The method of claim 14 in which the stripes that penetrate the well to the least extent are used to determine the location of the well.

16. The method of claim 15 in which the stripes of least extent that penetrate the two opposing edges of the well are used to determine the location of the two opposed edges.

17. A method of determining in a semiconductor wafer the location of two opposed edges that are of a well of conductivity type opposite that of the surrounding region and that underlie an insulating layer by forming over the surface of the wafer before forming of the well an overlay pattern of conductive stripes that

extend under the insulating layer to be formed and that comprise a first and second set of which at least one of the first set penetrates the well at the first of the opposed edges to form a low resistance connection to the well and at least one of the second set penetrates the well at the other of the opposed edges to form a low resistance connection to the well.

18. The method of claim 17 in which a voltage bias is applied in turn between pairs of stripes including one from each of the two sets for determining the pairs between which current flow is sufficient to establish penetration by each of an edge of the well.

19. The method of claim 18 in which each set includes stripes that penetrate on edge and stripes that do not penetrate and edge.

20. The method of claim 18 in which the stripes that extend into the well to the least extent from the first and second sets are used to determine the location of the opposite edges of the well.